Amendments to Specification

Please amend the specification at page 3, starting at line 4, to delete extraneous material as follows:

FIG. 1 depicts a high level block diagram of a signal analysis system;

FIG. 2 depicts a flow diagram of an analysis program ~~159~~ for separating the jitter components on a serial data stream suitable for use in the system of FIG. 1;

FIG. 3 depicts a flow diagram of the steps performed by the analysis program ~~159~~ in estimating the ISI + DCD versus data pattern;

FIG. 4 depicts a series of bits according to an embodiment of the present invention;

FIG. 5 depicts another series of bits according to an embodiment of the present invention; and

FIG. 6 depicts a flow diagram of the steps performed by the analysis program ~~159~~ in removing the ISI + DCD jitter from the serial data stream.

Also please amend the specification at page 4, starting at line 6, to correct a typographical error as follows:

A digitized output signal SUT' produced by the A/D converter 112 is stored in the acquisition memory 140. The acquisition memory 140 cooperates with the controller 150 to store the data samples provided by the A/D converter ~~110~~ 112

in a controlled manner such that the samples from the A/D converter ~~110~~ may be provided to the controller 150 for further processing and/or analysis.